FAULT-RESISTANT MANAGEMENT INFORMATION SYSTEMS FUNCTIONING IN THE MODULAR NUMBER SYSTEM

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The results of researches related to solving problems of improving the efficiency of real-time management information systems (MIS) functioning, obtained both in Ukraine and abroad, showed that the existing methods for improving the performance of information processing and fault tolerance of functioning, based on the use of binary position number system (PNS), do not always fully satisfy increasing requirements for special purpose information processing systems, which is caused by the following circumstances.

In the PNS, the quantitative value of each digit of the discharge depends on its place (position) in the original number. Any number is displayed as a sequence of digits of a given number system (NS). In MIS, the processes of performing arithmetic and logical operations on operands presented in a binary PNS in the form: $A = a_{\rho-1}2^{\rho-1} + a_{\rho-2}2^{\rho-2}$,..., $a_1 2 + a_0$, where $a_i = \overline{0,1}$ $(i = \overline{0,\rho-1})$.

The main difficulty in the implementation of arithmetic operations in the PSS is the organization of the process of formation and distribution of carry digits between the binary digits of the processed operands. The presence of interbit connections affects the process of error propagation, i.e. an error that occurs in one binary digit, in the process of transferring from low-order to high-order bits, propagates along the entire length of the machine word. The algorithmic connection in the PSS of all binary digits of the operands among themselves determines the fact that a single failure (failure) of the processing circuit of the binary digit of the operating device can cause not single, but multiple errors in the machine word.

Thus, a failure (failure) in the *i*-th circuit (Fig. 1) of processing the *i*-th binary digit during the formation of a partial sum *S* can occur in the following cases:

- in the process of forming the sum of operands *A* and *B*, one has to operate with three values - the digits of the first a_i and b_i second terms of the *i*-th digit, as well as the result c_{i-1} of the transfer to the given *i*-th digit from the lower $(i-1)$-th digit $(a_i, b_i, c_{i-1} \in \overline{0,1})$. $S_i = a_i \vee b_i \vee c_{i-1}$, i.e. an error occurs at the output of the processing circuit of the i-th binary digit [1];

- due to a failure (failure) in the transfer chains the value $c_{i-1} = (a_{i-1} \wedge b_{i-1}) \vee (a_{i-1} \vee b_{i-1}) \wedge c_{i-2}$, i.e. in the process of transferring the signal from the $(i-1)$-th processing circuit of the $(i-1)$-th binary digit to the input of the *i*-th processing circuit of the *i*-th binary digit; in this case, instead of the value $c-1$ is its inverted value, which generates an error in the processing circuit of the *i*-th binary digit, i.e. value is distorted c_{i+1} and S_{i+1} [2].

In addition, the algorithmic dependence of the content of binary digits and the need to take into account the size of the bit grid of existing MIS causes a significant duration of arithmetic operations (due to the need to wait for the end of the propagation of transfers over the entire length of the machine word).

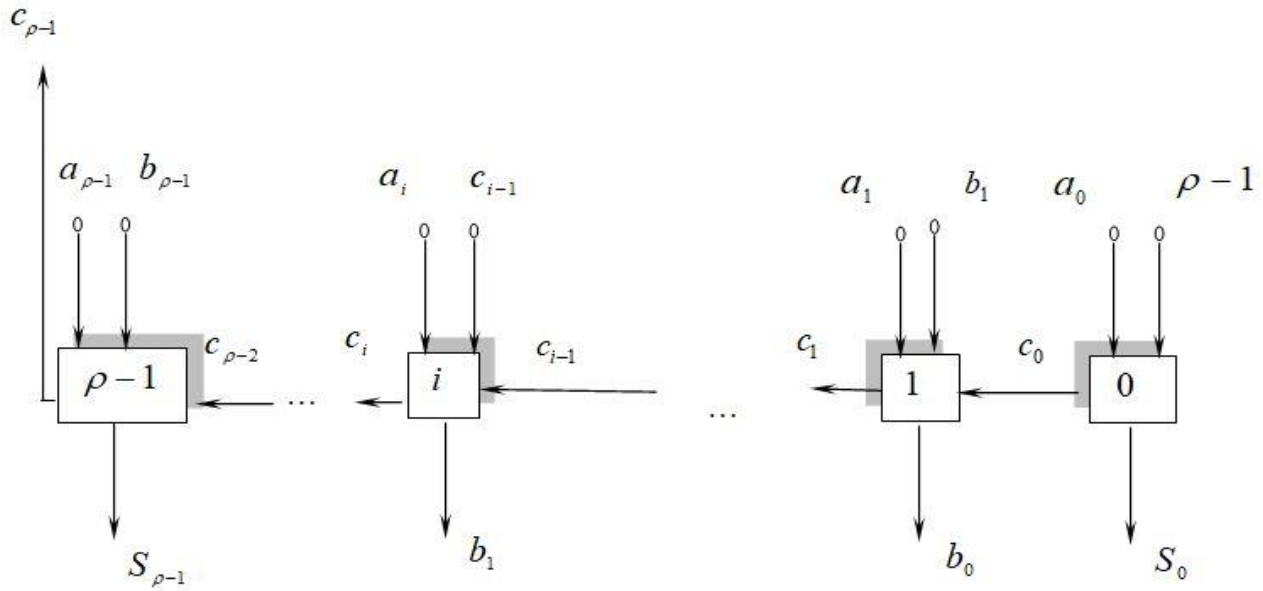

Figure 1. Block diagram of a binary positional adder

Also in the PNS, the time for the implementation of arithmetic operations depends on the length of the bit grid of the information processing device, which, in the context of the current trend in the development of MIS, aimed at increasing the length of the bit grid, is a limiting factor in improving the performance of such systems.

At the same time, methods for improving the performance of MISs operating in PNS have a common drawback - the inability to parallelize the algorithms being solved at the level of elementary operations (micro-operations), which is also primarily due to the presence of inter-bit connections in the PNS in the processed operands [3].

Development of a modern microelectronic base based on the use of large integrated circuits, programmable logic array (PLA) and field programmable gate array (FPGA), gave impetus to the study of the possibility of using tabular methods of information processing in the PNS. The use of these methods makes it possible to ensure high performance and reliability of the MIS, as well as a high degree of regularity and uniformity of the structure of devices for their implementation. A significant disadvantage of the tabular methods of information processing used in the PNS is significant hardware costs, which significantly complicates their practical implementation [4].

Thus, the main disadvantages of computing facilities operating in the PNS are low reliability and reliability of operation, a significant time for the implementation of arithmetic operations [5].

One of the possible ways to eliminate the shortcomings inherent in the PNS is to attract new original ideas in the field of machine arithmetic, which would make it possible to weaken or eliminate all interdigit connections.

Based on the fundamental concepts and provisions of the theory of comparisons, it was possible to create an original number system that can eliminate the indicated shortcomings, in which the number (operand) A is represented by a set $\{ a_i \}$ of the smallest residues from the successive division of the operand A by a set of mutually pairwise prime numbers $\{ m_i \}$, i.e. modular number system (MNS).

Note that the bases of the MNS are related to each other in such a way that they are chosen in a certain way and are fixed constant for a given MNS. Each modulo residue is informationally independent of other residues, but within each residue, when implementing information processing operations, a PNS is used (usually binary). Thus, MNS is correctly defined as a special construction of code numerical structures, i.e. a specially encoded block of information.

At $\prod_{i=1}^{n} m_i \geq A_k$ set of residues $\{a_i\}$ uniquely identifies the operand A_k and the numerical value of A_k becomes unnecessary, which makes it possible to implement modular operations on separate independent paths, operating only with the residues of $\{a_i\}$. Such coding of numbers allows you to create MIS, in which the processing of all digits of the number (residues a_i) is performed in parallel in time. In this case, the generalized block diagram of the information processing device in the MNS is a set of information processing paths (IPP) that operate independently of each other and in parallel in time, each with its own specific module m_i (Fig. 2).

In the IMS in the MSS, errors that occur due to failures (failures) of binary digit circuits in an arbitrary computing path do not “multiply” into neighboring paths (remain within one residue), which makes it possible to increase the reliability of calculations. In this case, it does not matter whether there was a single or multiple errors or a bunch of errors no longer than $[\log_2(m_i-1)]+1$ binary digits. An error that has arisen in the computational path of the MIS in the base mi is either stored in this path until the end of the calculations, or is eliminated in the process of further calculations. This property of the MNS allows you to create a unique system for monitoring and correcting errors in the dynamics of the computational process (without stopping the calculation process) of the MIS with the introduction of minimal code redundancy, which is essential for data processing systems operating in real time [6].

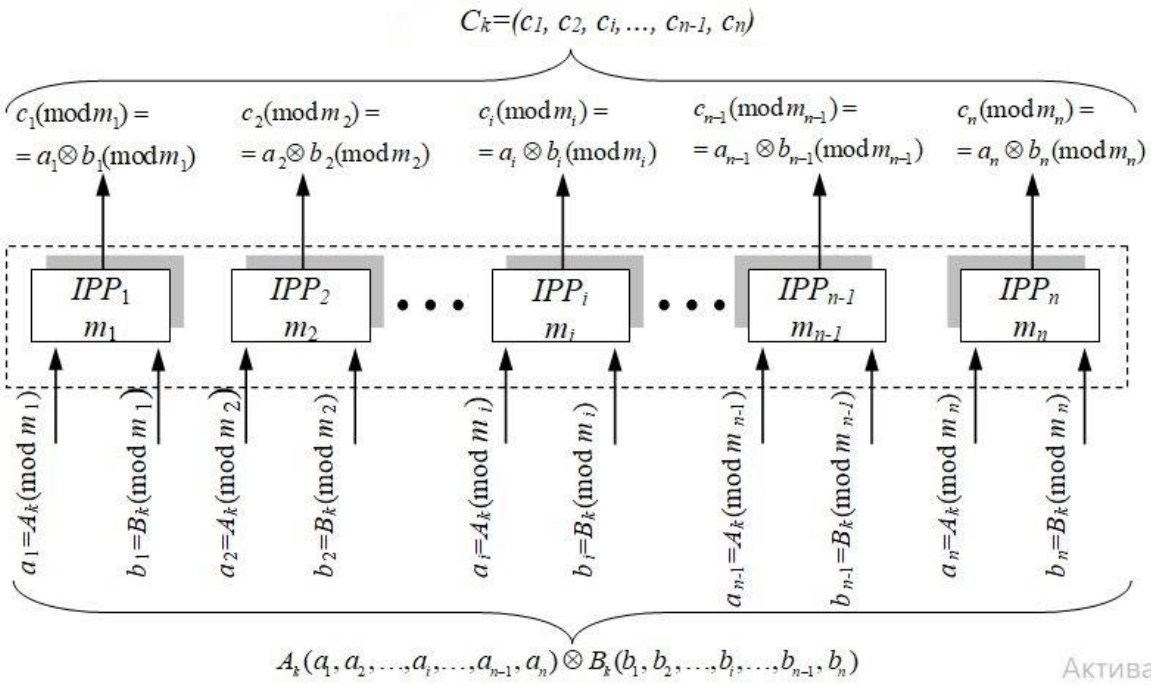

Figure 2. Structural diagram of the information processing device in the MNS

In addition to the fact that MNS allows you to meet high requirements for ensuring the fault tolerance of the functioning of the real-time MIS, also it is necessary to focus on the fact that the MIS in the MNS contains a slightly larger (by ≈15%) amount of equipment than the MIS in the PNS for a given equal length of the bit grid, without taking into account the introduction of secondary redundancy. However, as shown by theoretical studies and practical calculations, to ensure a given level of fault tolerance of the MIS in the MNS, a much smaller (up to 57%), depending on the size of the bit grid, the amount of additionally introduced equipment is required than for the MIS in the PNS.

References:

1. Akushsky I., Yuditsky D. Machine arithmetic in residual classes. Moscow, Sov. Radio, 1968, 440 p.

2. A. Yadin, Computer Systems Architecture. Chapman and Hall/CRC, 2016.

3. P. V. A. Mohan, Residue Number Systems. Cham: Springer International Publishing, 2016

4. Avizienis, A., A fault tolerance infrastructure for dependable computing with high-performance COTS components / A. Avizienis // Proc. DSN 2000, 30 th IEEE/IFIP Int. Conference on Dependable Systems and Networks, New York, NY, June 2000. - P. 492-500.

5. Hongbin LI, Qing Zhao, Zhenyu Yang. Reliability modeling of fault tolerant control systems Int. J. Appl. Math. Comput. Sci., 2007, Vol. 17, No. 4. – P. 491-504.

6. Ulman Z. Sign detection and implicit conversion of number in residue arithmetic / Z. Ulman // IEEE Trans. Comput. – 1983, Vol. C-32, № 6. – P. 590-595.