УДК 681.04

***Янко А.С.**, к.т.н., доцент кафедри комп'ютерних та інформаційних технологій і систем, Навчально-науковий інститут інформаційних технологій і механотроніки, Національний університет «Полтавська політехніка імені Юрія Кондратюка», 0000-0003-2876-9316, al9_yanko@ukr.net*

ТАБЛИЧНИЙ МЕТОД РЕАЛІЗАЦІЇ АРИФМЕТИЧНИХ ОПЕРАЦІЙ У СИСТЕМІ ЗАЛИШКОВИХ КЛАСІВ

***Анотація.** Основною метою цієї статті є, по-перше, ознайомлення аудиторії та спеціалістів, які не знайомі з основами системи залишкових класів (СЗК). По-друге, дати уявлення про сучасний стан розвитку СЗК у світі, і, нарешті, по-третє, показати можливі перспективні методи підвищення користувальницької продуктивності комп'ютерних систем та компонентів швидкої обробки цілочисельних даних (КСКШОЦД) в режимі реального часу, завдяки використанню властивостей СЗК і на цій основі принципів здійснення арифметичних операцій в СЗК. Малорозрядність залишків забезпечує можливість реалізації табличної арифметики, при якій результат операції не обчислюється кожен раз, а після обчислення поміщається в запам'ятовуючий пристрій (пам'ять) і при необхідності зчитується з нього, тобто здійснюється за один період синхронізації частоти (машинний такт). Табличний метод в СЗК може виконувати не тільки найпростіші операції, але й складні функції за один машинний такт. Це визначає одну з парадоксальних властивостей СЗК: ефективна продуктивність модульної комп'ютерної системи може бути значно вищою у кілька разів, у десятки і сотні разів, ніж позиційна двійкова комп'ютерна система з тією ж тактовою частотою. Дійсно, операцію, яку звичайні КСКШОЦД виконують за 100 тактів, модульні КСКШОЦД виконують за один такт, звичайно, їх ефективна продуктивність виконання цих операцій у 100 разів вища.*

***Keywords:** принцип суматора, регістри кільцевого зсуву, комп'ютерні системи та компоненти швидкої обробки цілочисельних даних, операційний пристрій, принцип кільцевого зсуву, система залишкових класів, табличний принцип.*

UDC 681.04

***Yanko A.**, PhD, Associate Professor of the Department of Computer and Information Technologies and Systems of the Educational-scientific institute of information technologies and mechanotronics of the National University «Yuri Kondratyuk Poltava Polytechnic», 0000-0003-2876-9316, al9_yanko@ukr.net*

TABULAR METHOD OF THE IMPLEMENTATION OF ARITHMETIC OPERATIONS IN THE SYSTEM OF RESIDUAL CLASSES

***Abstract.** The main goal of this article is, firstly, to familiarize the audience and specialists who are not familiar with the fundamentals of the system of residual classes (SRC). Secondly, to give an idea of the current state of the development of SRC in the world, and, finally, thirdly, to show possible promising methods to improve user productivity of computer systems and components of fast processing of integer data (CSCPID) real time, through the use of the properties of the SRC and on this basis the principles of implementation of arithmetic operations in SRC. The small bitness of the residuals provides the possibility of implementing tabular arithmetic, in which the result of the operation is not calculated every time, but once calculated it is placed in a storage device (memory)*

and, if necessary, read from it, i.e. one period of synchronizing frequency (machine clock).The tabular method in the SRC can perform not only the simplest operations, but also complex functions, and also in one machine cycle. This determines one of the paradoxical properties of the SRC: the effective performance of a modular computer system can be significantly, several times, tens and hundreds of times higher than that of a positional one with the same clock frequency. Indeed, the operation that a regular CSCPID performs in 100 cycles, the modular CSCPID performs in one cycle, of course, its effective performance on these operations is 100 times higher.

Keywords: *adder principle, circular shift registers, computer systems and components of fast processing of integer data, operational device, principle of circular shift, system of residual classes, tabular principle.*

The use of the property of small digits of residues in the representation of numbers in the SRC provides a wide choice of system-engineering solutions when implementing modular operations. It is known that there are four principles for the implementation of arithmetic operations in the SRC: adder principle (AP) (based on low-bit binary adders); tabular principle (TP) (based on the use of ROM; direct logical principle of implementation of arithmetic operations based on the description of modular operations at the level of switching functions systems, by means of which the binary digits values of the resulting deductions are formed (it is advisable to use systolic values for the technical implementation of this principle) and programmable logic arrays, as well as FPGAs); the principle of circular shift (PCS), based on the use of circular shift registers (CSR).

The absence of inter-bit connections between binary digits of an operational device (OD) of an information processing system in the process of implementing modular operations based on TP or PCS is one of the main and most attractive features of the SRC.

In the positional number system, the execution of an arithmetic operation involves sequential processing of the bits of the operands according to the rules determined by the content of this operation and cannot be completed until the values of all intermediate results are consistently determined taking into account all connections between the bits [1, p. 12]. Thus, PNS, in which information is presented and processed in modern CSCPIDs, have a significant drawback - the presence of inter-bit connections, which leave their mark on the methods of implementing arithmetic operations, complicate the equipment, reduce reliability and limit speed. Therefore, it is natural to search for possibilities of constructing such arithmetic, in which the bit connections would be absent. In this regard, the number system in the residual classes attracts attention. The system of residual classes has the valuable property of independence of residuals from each other according to the adopted system of bases. This independence opens up broad possibilities in building not only new machine arithmetic, but also a fundamentally new implementation of CSCPIDs, which in turn significantly expands the use of machine arithmetic. The number system to a greater extent affects the structure of the operating device of CSCPID.

Fundamentally, the CSCPID operational device in the SRC can be executed either in the adder variant (based on low-bit binary adders) or in the tabular (matrix) variant. When constructing an OD on the basis of low-bit adders, each of the digits of the number is processed independently, but the execution time of the entire operation is determined by the time required to obtain the result on the largest base of the SRC [2, p. 77].

Note the main disadvantages of the adder version of the implementation of arithmetic operations:

- the complexity of the synthesis of binary adders;
- large information conversion time for significant CSCPID bit grids, determined by the maximum base of the SRC;
- the complexity of the multiplication operation;

inefficient use of binary elements of OD of the CSCPID, due to the redundancy of the maximum numbers that can be represented by adders, compared with the values of the bases of the SRC;

- low reliability of calculations due to errors arising in the process of calculations and at the expense or in the process of transfers of intermediate values of bitwise summation.

The schematic implementation of the SRC, as in general, the schematic implementation of any

number system is determined not only by the logical specifics, but also by the equipment used and the organization of this equipment. A big reserve of increasing the reliability of CSCPID is the use of matrix schemes of ROM, PLM and FPGA in the OD. Low power consumption, increased reliability characteristics of matrix machines open up wide prospects for their use as the main elements of OD of CSCPIDs. From the conducted research it is obvious that the issues related to the performance of arithmetic operations using tabular methods (by means of ROM) are advisable to be considered only in application to CSCPIDs in the SRC. The question of which method allows us to get the least amount of equipment is not straightforward. When using methods of special coding information in the SRC, the purpose of which is to reduce the OD tables that implement arithmetic operations, the quantity of OD equipment in a tabular construction can be no more than the amount of equipment in the summation method of constructing the OD of CSCPID in the SRC. The advantages of the tabular version of the construction of the OD of CSCPID in the SRC:

- matrix circuits have a fairly high reliability, since they are implemented in the form of compact ROMs; in this case, the entire path of the OD of CSCPID is built according to the block principle, which improves the maintainability of the CSCPID (reduction of the recovery time $T_в$);

- the simplicity of the matrix circuits and decoders having a number of outputs corresponding to the base of the SRC;

- high speed; the result of the operation can be obtained at the moment of receipt of input operands, i.e. in one clock cycle; the execution time of arithmetic operations in the SRC is comparable to the clock frequency of the calculator, which is fundamentally impossible for positional computers with the existing element base [2, p. 78].

The search for ways to simplify the structure of CSCPIDs necessitated the construction of algorithms for implementing modular operations, which make it possible to increase the efficiency of using tabular arithmetic.

Let a pair of operands $A=(a_1,...,a_n)$ and $B=(b_1,...,b_n)$ in the SRC be given with pairwise mutually simple bases. It is necessary to implement in a tabular version a generic modular operation $(A\otimes B)\bmod M$. In accordance with the rules for performing arithmetic operations, for each pair of residuals a_i and β_i is assigned a value $(a_i\otimes b_i)\bmod m_i$. Thus, the entire machine path of a computational operation $(A\otimes B)\bmod M$ can be represented as independent, single-type ROMs [3, p. 147].

In the general case, if it is necessary to process information in the complex area with an increase in the rate $N=p^2+q^2$ of the module of the modular operations table (for a module $(m=p+iq)$) it becomes cumbersome, which naturally leads to an increase in the equipment of the computing device and affects the time for the implementation of arithmetic operations. On the basis of this great theoretical and practical interest represents the task of informational compression of the contents of the matrices of the main modular operations in the SRC. This task is closely connected with the development of how special design and synthesis of special algorithms that improve the structure of modular tables, and with the formulation, development and application of new principles, methods and algorithms for the implementation of arithmetic operations.

A relatively significant amount of CSCPID equipment during its implementation on the basis of the TP, as well as its significant mass-dimensional characteristics, limits the scope of its use in some specialized automated control systems. In this aspect, it is necessary and important to study the ways of using other information processing principles in the real-time CSCPIDs operating in SRC.

If the TP and methods of its implementation are well known and rather deeply studied, then the PCS was proposed relatively recently, so for its wide use it is necessary to solve a number of problems related to the choice of a rational structure of CSCPID, which in turn is directly related to the development and the use of methods and algorithms for processing information in the SRC based on PCS.

In the positional number system, the execution of arithmetic operations involves the sequential processing of the bits of the operands according to the rules of this operation and it cannot be completed until the results of the inter-bit operations are determined consistently with all the links

between the bits. Thus, the PNS used in modern computers, in which information is presented and processed, has a significant drawback - the presence of inter-bit connections, which leave their mark on the principles of implementation of arithmetic operations.

The system of residual classes, as noted above, has the valuable property of independence of residues from each other according to the adopted system of bases. This opens up broad possibilities in building not only new machine arithmetic, but also in a fundamentally new circuit implementation of CSCPID, which, in turn, significantly expands the use of machine arithmetic.

The CSCPID operating device in the SRC can be implemented either in a adder version (based on low-bit binary adders), or in a tabular (matrix) version. When constructing an OD on the basis of small-bit adders, each of the number digits is processed independently, but the execution time of the entire operation is determined by the time required to obtain the result on the largest base of the SRC.

Note the main disadvantages of the adder version:

- some complexity of the synthesis of binary adders;
- long time of information transformation, determined by the value of the maximal base of the SRC;
- the complexity of the multiplication operation; inefficient use of binary elements of the CSCPID digit grid due to redundancy in the representation of maximum numbers.

The reserve for improving the reliability and performance of CSCPID is the use of matrix circuits based on permanent memory devices (ROM) in the OD. The low power consumption and the increased reliability characteristics of matrix circuits open up broad prospects for their use as the main elements of the OD.

It is obvious from the conducted studies that issues related to the performance of arithmetic operations using tabular methods (via ROM) are advisable to be considered only when applied to CSCPID in the SRC.

The advantages of the matrix version of the construction of CSCPID in the SRC:

- matrix circuits have high reliability, since they are implemented in the form of compact ROMs; in this case CSCPID is built on the block principle, which improves its maintainability (in particular, the average recovery time is reduced);
- simplicity of matrix circuits and decoders having a number of outputs, which corresponds to the size of the base of the SRC;
- high speed: the result of the operation can be obtained at the moment of receipt of input operands, i.e. in one measure; thus, the time of performing arithmetic operations in the SRC is comparable to the clock frequency of the calculator [2, p. 80].

When applying methods of special coding of information in the SRC, (the purpose of which is to reduce the elements of the tables of elements of the ROM), which implement arithmetic operations, it can be achieved that the quantity of OD equipment in a tabular construction can be no more than the quantity of equipment with the summation principle the construction of CSCPID OD in the SRC.

Consider the methods and algorithms that allow you to effectively perform modular operations of multiplication, addition and subtraction, using the tabular principle of implementing arithmetic operations [4, p. 24].

References

1. I.Ya. Akushskii and D.I. Yuditskii, "Machine Arithmetic in Residual Classes [in Russian]," Sov. Radio, Moscow, 1968.

2. V. Krasnobayev, A. Kuznetsov, A. Yanko, S. Koshman, A. Zamula and T. Kuznetsova. Data processing in the system of residual classes. Monograph. ASC Academic Publishing, 2019, 208 p. – ISBN: 978-0-9989826-6-3 (Hardback), ISBN: 978-0-9989826-7-0 (Ebook).

3. V. Krasnobayev, A. Yanko and S. Koshman, "A Method for arithmetic comparison of data represented in a residue number system," Cybernetics and Systems Analysis, vol. 52, Issue 1, 2016, pp. 145-150.

4. R. F. Hodson, Real-Time Expert Systems Computer Architecture. CRC Press, 2018.